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A Reduced Switch Multilevel Inverter Topology Utilizing a Capacitive Divider

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Abstract— **A reduced switch multilevel topology which can be used for intermediate power drive applications is presented in this paper. The multilevel converters give high level voltages by reducing the harmonics in the waveform. The harmonic content of the output wave decreases in proportion to the number of levels. The high frequency switching in conventional adjustable speed drives give rise to motor bearing failure with high switching losses. In H-bridge topology, additional dc sources are needed with increase in number of levels. This paper introduces a reduced switch multilevel topology which possess a capacitor divider in parallel to source and an input diode in series with the source offering additional advantage of reduction in power electronic switches. This new topology uses only five main switches and a single diode for the working of a five- level inverter. Again the working of a five level inverter using the proposed topology has been studied and simulated. The hardware implementation and simulation of five level inverter has also been done.**

Keywords—**H-bridge, five-level inverter, capacitive divider.**

I. INTRODUCTION

bearing failure due to high transient voltages.
─high sw A number of drawbacks can be depicted in relation to conventional adjustable speed drives such as
─ as motor itching frequency accompanied with switching losses.

The multilevel converters [2] reduce the voltage stress to the main power switches by operating at various voltage levels. Conventional multilevel inverters can be broadly classified under three different topologies: diode clamped, capacitor clamped and cascaded multilevel inverter with more attractive features. According to the requirement various modulation strategies has also been proposed such as multilevel sinusoidal pulse width modulation [9], multilevel selective harmonic elimination and space vector modulation. In the case of a diode clamped multilevel inverter [2] showed in Fig.1, the two diodes aids in attaining half level voltages. But the number of uncontrolled switches is a problem with the diode-clamped topology. This topology is mostly used for statcom [2] based applications. Each of the topologies has got it's own advantages and disadvantages. A detailed analysis of each of the above three basic topologies is mainly based on the different switching states of the multilevel inverter.
A capacitor clamped inverter is however more flexible than a diode clamped inverter. The capacitor with positive sign is in discharging mode and that with negative sign in charging mode. The balancing of the capacitor charge is made possible by proper selection of the capacitor combinations. The requirement of a large number of bulky capacitors to clamp the voltage is yet another disadvantage. So to compensate the disadvantages of diode clamped and flying capacitor inverters, cascaded multilevel inverters [3]-[4], [10] were introduced. It consists of a modularised circuit design and hence this topology is used in most of the practical purposes. The main advantage of pwm converters [9] in power electronics is the reduction of harmonics and passive component sizes by operating at increasingly high frequencies. However the switching losses increase as the switching frequency increases which becomes significant at higher frequencies. All the above multilevel topologies reduce these switching losses by operating at very low frequencies. As more levels are added to the multilevel inverter, it is able to synthesize better waveforms [5]. In paper [1], [6]-[7] the reduction in number of switches and power devices is attained by a new topology. Even though the multilevel converters are widely used for high power drive applications, here for convenience it is being tested for single phase only.

II. PROPOSED TOPOLOGY

A. Circuit Configuration

An H-bridge using new topology with an input diode is shown in the Fig.1. The controlled switch S_5 with antiparallel diode acts in conjugation with main switches act to get the maximum voltage levels. To compensate the disadvantages of conventional adjustable speed drives, the new topology is being proposed. Here a considerable saving in the number of main switches is achieved. Comparing with the conventional five-level inverter with eight switches, the proposed topology employs only five switches which makes it more suitable for drives application.

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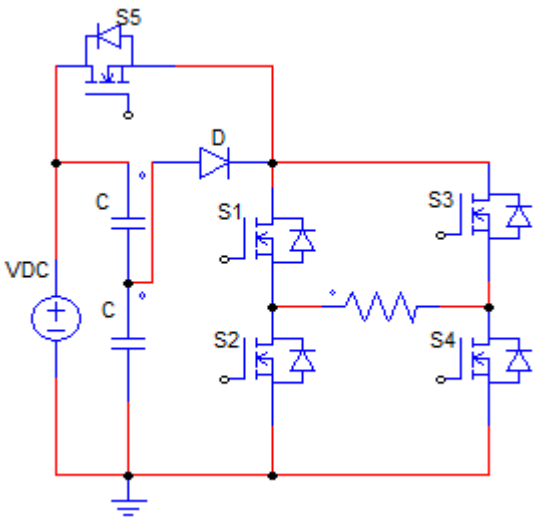


Fig. Circuit Diagram for proposed topology

B. Power Stage Operation

The five different output voltage levels (V_S, $V_S/2$, 0, $-V_S/2$, $-V_S$) are generated as shown in the corresponding five figures. For getting maximum positive output of V_S switches S_1, S_2 and S_5 are kept on keeping all other controlled switches off. For getting half level positive output of $V_S/2$, the switch S_1 is in the on position with switch S_2.If all other controlled switches are off, the voltage applied across the load will be half level positive output $V_S/2$.The path for current is shown in the Fig.5. To get a zero voltage level, all the switches are turned off and there will be no voltage applied across the circuit load making the output voltage zero.

Modes	Switching Pattern					
	V_O	S_1	S_2	S_3	S_4	S_5
Mode-1	V_S	1	1	0	0	1
Mode-2	$0.5V_S$	1	1	0	0	0
Mode-3	0	0	0	0	0	0
Mode-4	$-V_S$	0	0	1	1	1
Mode-5	$-0.5V_S$	0	0	1	1	0

TABLE-1:Switching pattern for proposed inverter

To produce a half level negative output of $-V_S/2$ for five level inverter, switch3 is on together with switch4 to connect load negative to V_S.. For getting maximum negative voltage switches 3 and 4 are on together with switch5 keeping all other switches off. Capacitors in series are directly connected in parallel to the dc source. So to restore the voltage balance in capacitors is not a problem for the proposed topology. Compared to standard multilevel converters the overall cost of the proposed topology will be reduced.

C. Simulated Resullts

Fig.12 and Fig.13 shows the simulated output voltage and harmonic spectrum for five level inverters. Fundamental output frequency is 50 Hz. The five voltage levels in the figure are 100V, 50V, 0V, -50V and -100V for a dc voltage source of 100V. The proposed circuit when simulated in MATLAB/SIMULINK produce a THD of 24.36%.

Fig. 1 FFT Spectrum for proposed topology

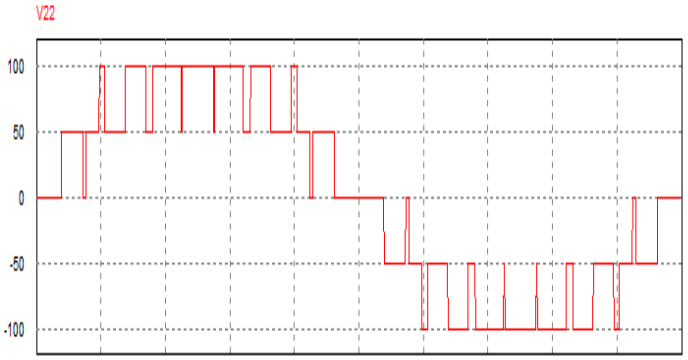
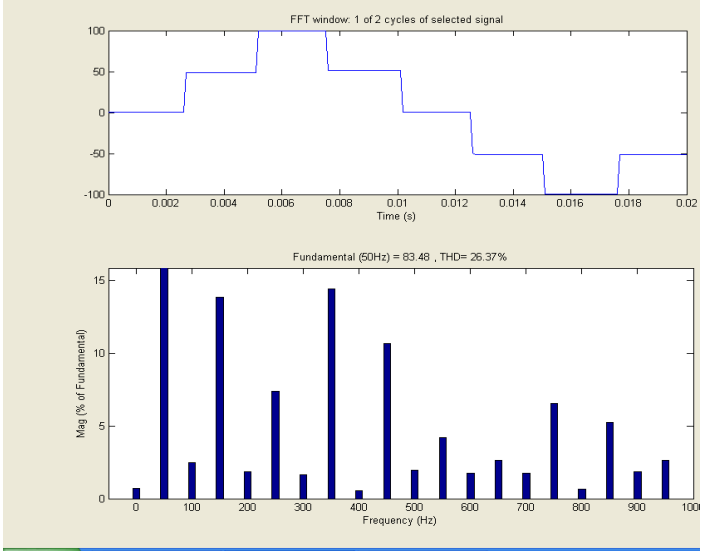


Fig. 2 Simulated output voltage for proposed five-level inverter



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D. Experimental set up

The experimental set up of five level inverter has been done using Arduino Uno. The hardware specifications are tabulated in the form of Table-2. The output voltage of five-level inverter is given by Fig. 13. The experimental set up for proposed topology is shown in fig.

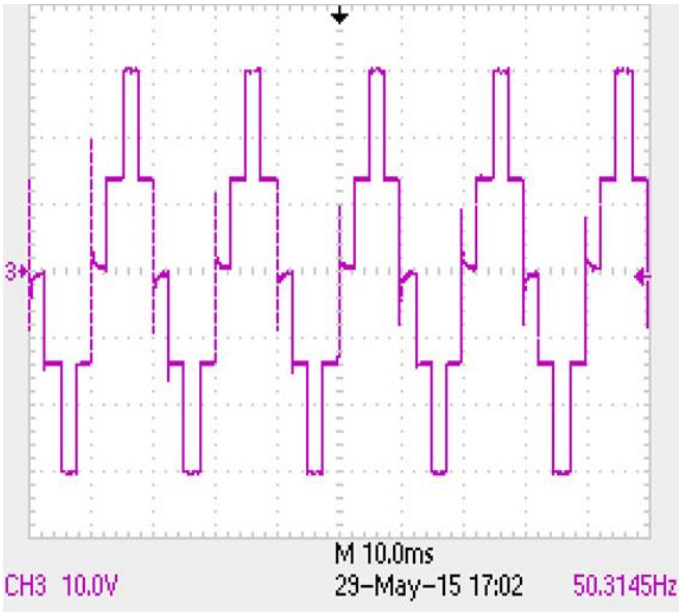
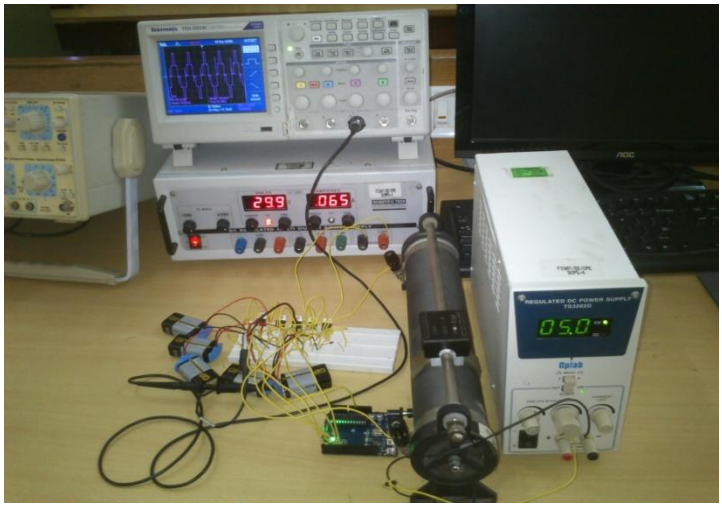


TABLE 2: Hardware Specifications

Output Frequency	50 Hz.
Input Voltage	30Volt(Dc)
Output Voltage	21.22 (rms)
Output Power	1.164 W
Mosfet	IRF540
Capacitors	15V, 1W
Load resistance	50Ω
Load Inductance	Nil



A. Conclusions and future scope

From the simulation results it is shown clearly that the proposed topology with reduced switches works as expected. The circuit explanation for the new inverter with induction motor load has been made and simulated. By using adequate filter circuits, the THD can be further reduced.. Even though this new topology can be used for drives applications, here it is tested for single phase only. The proposed circuit can be extended to three phase systems also.

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